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Implementation of noise-aided logic gates with memristive circuits

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Abstract. We implement robust logic gates utilizing a second order autonomous memristive circuit in the presence of a noise floor. We find that extremely reliable operations are obtained in an optimal band of moderate noise, with both direct and complementary logic operations obtained in parallel. The system also has the capacity to morph between logic functions efficiently by a simple change of bias, laying the foundation for noise-aided reconfigurable logic gates. Lastly, we implement coupling induced logical stochastic resonance (LSR) on a coupled system of memristors, paving the path for the realization of multi-input logic gates without the need for separate adder circuits. All ideas are demonstrated explicitly through numerical simulations, as well as proof-of-principle circuit experiments. Thus, our results suggest that the memristive circuit offers a promising system to implement robust and flexible logic operations in noisy environments and may help expand the scope of memristive device-based memcomputing.

Keywords. Logic gates; memristive circuits; logical stochastic resonance.

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1. Introduction

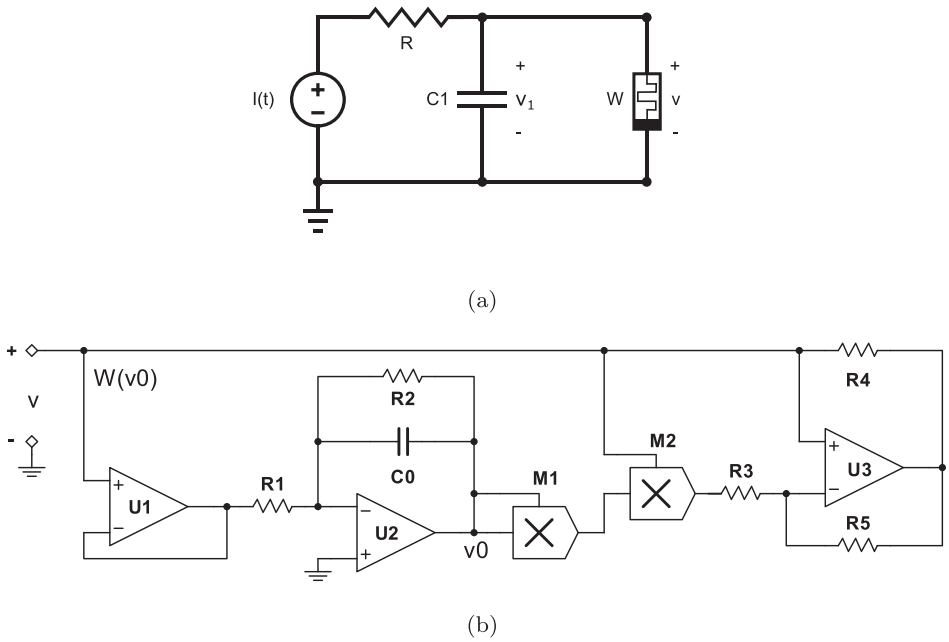
In an exciting new development, that has drawn wide research interest, it was demonstrated that a bistable system driven by the sum of two external signals consistently functioned as a logic gate in a window of moderate noise [1]. This phenomenon, termed *logical stochastic resonance* (LSR), has been successfully realized in systems ranging from electronic circuits [2–5], nanomechanical devices [6], Coulomb-coupled quantum dots [7] and optical systems [8, 9], to chemical systems [10] and bio-inspired systems such as synthetic genetic networks [11–17]. In this work we expand the scope of this phenomena by implementing noise-aided logic gates with a memristive circuit, i.e. circuits built of resistors with memory.

Memristive devices (memristors) are used principally for resistive switching memories, and these have been considered very promising candidates for developing novel state-of-the-art memory technology. Moreover, it has been established that networks of memristors may potentially help implement neuromorphic computing architectures [18, 19]. The main advantages of computing with memristive elements are their low power consumption and their ability to store and process information on the same physical platform, and memristive devices thus promise powerful alternatives to conventional computing platforms [20]. So our central aim here is to provide a proof-of-principle illustration that a memristive circuit is a promising system for implementing robust and flexible noise-aided logic operations. This pushes forward the potential of memristive devices in general and offers directions for expanding the scope of memcomputing.

2. LSR using memristive circuit

Specifically, we have used a second order autonomous memristive circuit from Ref. [21] to implement LSR. In figure 1a we display the schematic of the circuit, which consists of a resistor, capacitor and memristor. We have used a simple, inductor-free equivalent circuit to emulate the memristive behaviour, as shown in figure 1b. Since the memristive circuit considered in this work is inductor-free, it makes the circuit comparatively much simpler and more suitable for future IC design.

The dynamics of this circuit is dictated by two components, the capacitor C_1 and active voltage controlled memristor with memductance $W(v_0)$. Hence



(a)

(b)

Figure 1. (**a**) Schematic of the single memristor-based circuit. (**b**) Equivalent circuit of the memristor W. The multipliers (M1 and M2) are realized with AD633. The op-amps U1, U2, and U3 are realized with AD712. The circuit parameters are fixed as $R_1 = 8$ kΩ, $R_2 = 4$ kΩ, $R_3 = 1.4$ kΩ, R_4, $R_5 = 2.2$ kΩ, $C_0 = 5$ nF, $g = 1$ V^{-2}, $R = 3$ kΩ and $C_1 = 10$ nF.

the circuit maybe modelled with voltage v_1 across capacitor C_1, and voltage v_0 as shown in figure 1, as the two state variables. This yields the governing equations:

$$\frac{dv_1}{dt} = \frac{I(t) - v_1}{RC_1} + \frac{(1 - gv_0^2)v_1}{R_3C_1},$$
$$\frac{dv_0}{dt} = -\frac{v_1}{R_1C_0} - \frac{v_0}{R_2C_0}, \quad (1)$$

where $I(t)$ is the combined input given to the system and is the sum of input streams I_1 and I_2, noise $D\eta(t)$ and bias b, i.e. $I(t) = I_1 + I_2 + D\eta(t) + b$. The noise term $\eta(t)$ is a zero mean δ-correlated Gaussian noise, with variance 1 and D is the noise strength. The focus of our investigation here is the switching of the states of the system under varying noise strengths, and different bias parameters, and ascertaining whether this emergent switching can yield consistent logic outputs [22].

2.1 Computational model

In order to computationally model the system we use the non-dimensionalized form of eq. (1)

$$\dot{x} = f_x(x, y) = -x + \alpha_1 x(1 - gy^2) + I(t),$$
$$\epsilon\dot{y} = f_y(x, y) = -\alpha_2 x - \alpha_3 y. \quad (2)$$

The output is determined by the sign of variable x (or y). For instance, we can assign logic output value 1 to $x(t) > 0$, and output value 0 to $x(t) < 0$. Assigning output value 1 to negative $x(t)$, and output value 0 to positive $x(t)$ will yield the *complementary logic operation*.

Figure 2 shows the time-series of the two variables $x(t)$ and $y(t)$ for the corresponding input sequence I_1 and I_2, with bias $b = +1$. We see that *consistent logic output* is obtained for *moderate noise* at $D = 1$ and the reliability of the logic response is lost for both low noise strengths (for instance, $D = 0.4$) and high noise strengths (for instance, $D = 2.5$). Specifically, state variable $x(t)$ consistently produces an OR logic output, while the other state variable $y(t)$ produces the complementary NOR logic output, *in parallel*.

Most interestingly, given that both the signals are sub-threshold at $I_1, I_2 = \pm 1$ the logic response is considerably *amplified*. For the parameters used here, the response from $y(t)$ is *double* that of the input streams and $x(t)$ is *five* times that of the input streams.

Further, the bias b is the control parameter that determines the nature of the logic function being implemented. For instance, in this system when bias b takes value +1 one obtains a OR/NOR logic gate, and when it takes value -1 one obtains a AND/NAND logic gate. So a simple change of the bias allows us to morph between fundamental logic functions and lays the building block for potentially reconfigurable computing devices.

2.2 Experimental verification

We verify the computational results by constructing the circuit shown in figure 1. The time traces of the voltage across capacitor C_1 for different values of noise

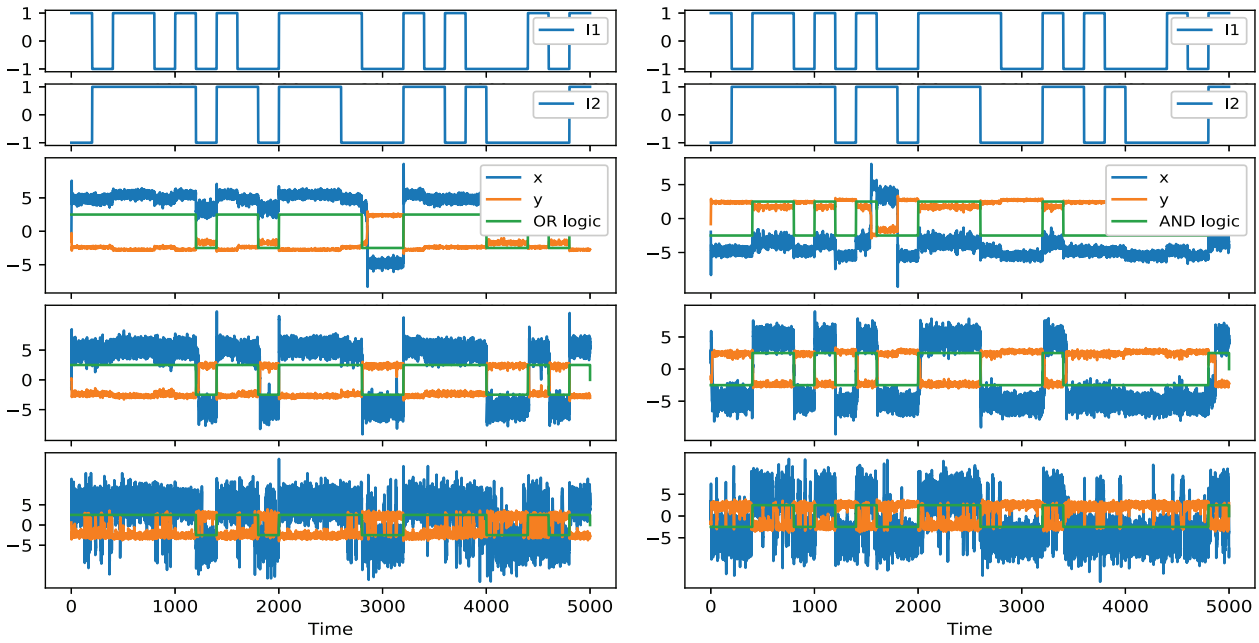
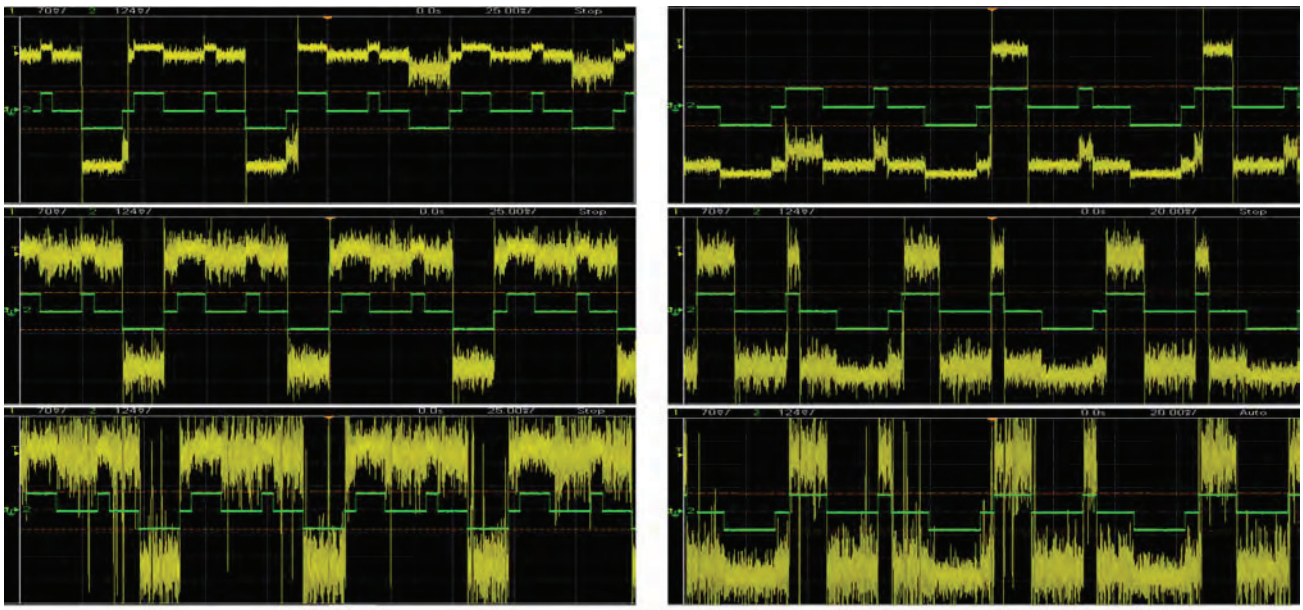


Figure 2. Time-series of variables $x(t)$ and $y(t)$ obtained by simulating eq. (2), for three values of noise strength D, $D = 0.4$, $D = 1$, $D = 2.5$, with bias $b = +1$ yielding OR/NOR logic (left) and $b = -1$ yielding AND/NAND logic (right). The corresponding input streams I_1 and I_2 are also shown. Here $x(t) > 0$ (or $y(t) > 0$) corresponds to logic output 1 and $x(t) < 0$ (or $y(t) < 0$) corresponds to logic output 0. The parameter values used for the simulation are $g = 0.1$, $\alpha_1 = 1.86$, $\alpha_2 = 0.325$, $\alpha_3 = 0.65$ and $\epsilon = 0.69$.



(a) (b)

Figure 3. Waveforms obtained from hardware implementation of the memristive circuit, for different noise levels: $D = 500$ mV (top) $D = 1.5$ V (middle) and $D = 2.5$ V (bottom); noise bandwidth 10 kHz (cf. figure 1b). The panels also show the sum of the two input streams $I_1 + I_2$ (green). I_1 and I_2 take value -0.5 V when logic input is 0 and value +0.5 V when logic input is 1. Here the bias b is set to (**a**) $b = +250$ mV_{pp} and (**b**) $b = -250$ mV_{pp}. Clearly the middle panel (moderate noise) yields a consistent OR logic output for (**a**) and AND logic output for (**b**). The noise signal is drawn from Agilent or Keysight 33522A, Function/Arbitrary Waveform Generator. The oscilloscope used is Agilent or Keysight DSOX2012A. The scale of the traces is 70 mV/Div (Y-axis) and 25 mS/Div (X-axis).

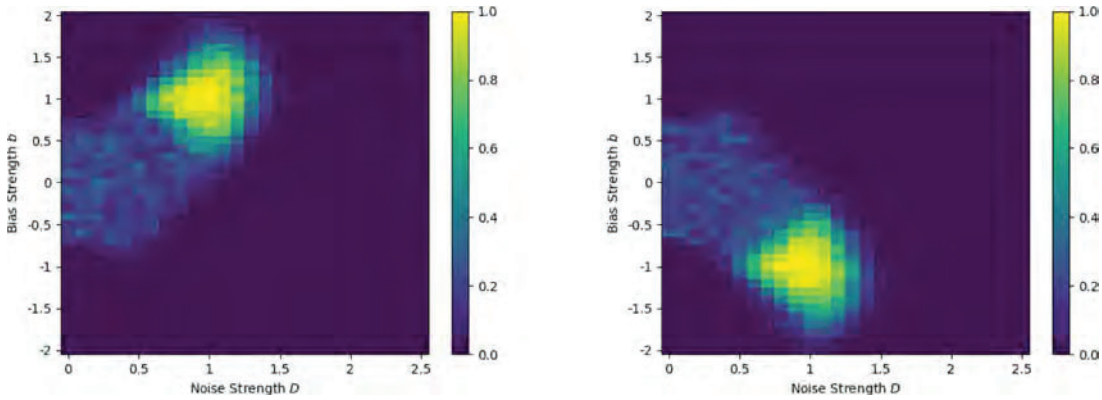


Figure 4. Dependence of the probability of obtaining (left) OR logic operation, P(OR) and (right) AND logic operation P(AND), on noise strength D and bias b, for system parameters: $g = 0.1$, $\alpha_1 = 1.86$, $\alpha_2 = 0.325$, $\alpha_3 = 0.65$ and $\epsilon = 0.69$ in eq. (2).

strength D and bias b are shown in figure 3. We see that consistent logic is obtained only in the presence of a moderately strong noise. Further, note that the response time of the system is very short, with the system taking of the order of microseconds on average to switch between the desired states, leading to low latency.

2.3 Quantitative measure of reliability

A quantitative measure of how reliably this system performs logical operations is obtained by comparing the output of the system with the expected logical output, over long times, and for different input sets. The probability of obtaining the desired output is estimated by driving the system with a stream consisting of a large number of (I_1–I_2) sets, where each run consists of the four input sets (0, 0), (0, 1), (1, 0), (1, 1), in different permutations. So the memristive system is subject to many different random combinations of I_1 and I_2 over time and its response to this random stream of inputs is recorded. If the logic output, as obtained from $x(t)(y(t))$, matches the logic output in the truth table for *all* input sets in the run, it is considered a success. The probability, P(logic), is the ratio of the number of such successful runs to the total number of runs sampled. The fraction of time where one obtains the desired logic output successfully, gives a measure of the probability of obtaining that specific logic, denoted as P(OR) or P(AND). When this measure approaches 1 we have completely reliable logic outputs. In figure 4 we show this measure, and it is clearly evident that there is an optimal window of noise strength D, for which AND/NAND and OR/NOR logic is consistently obtained. Similar behaviour is obtained for OR logic, as also displayed in figure 4.

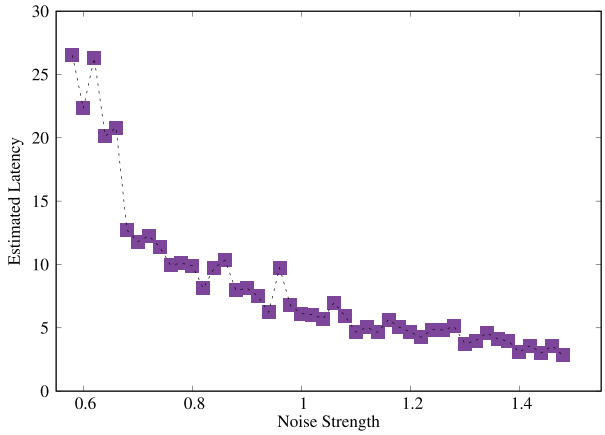


Figure 5. Estimated latency as a function of noise strength, where P(OR) $\sim$ 1. Here latency is estimated from numerical simulations and is the transience time taken to reach the desired output when an input switches, averaged over a random stream of inputs. It is shown in terms of the scaled time in eq. (2), where 1 unit of scaled time is 24 microseconds. The system parameters are those given in figure 4, with bias $b = 1$. Similar results are obtained in the noise window where P(AND) $\sim$ 1, with $b \sim -1$.

We also observed the reduction of latency with increasing noise. This can be seen clearly from the representative results displayed in figure 5. It is evident that the system responds to inputs faster when noise intensity is higher. So the desired hopping between wells happens more rapidly under the influence of stronger noise. This is yet another feature where noise assists performance.

3. Coupling induced LSR using memristive circuit

In recent work, the behaviour of coupled bistable subsystems subject to noise from two independent uncorrelated noise sources, over a range of coupling and noise

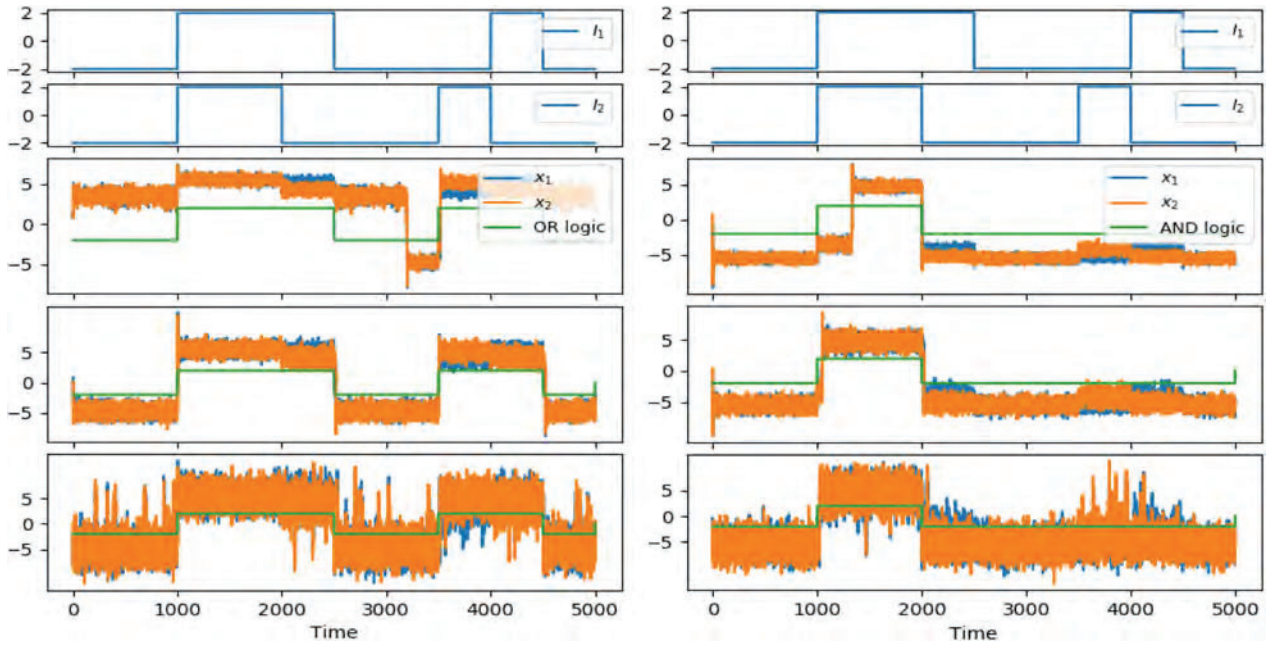


Figure 6. Time-series of variables $x_1(t)$ and $x_2(t)$ obtained by simulating eq. (3), for three values of noise strength D, $D = 0.5$, $D = 1$, $D = 2.5$, with bias $b = +1$ yielding OR/NOR logic (left) and $b = -1$ yielding AND/NAND (right) logic. Coupling strength $c = 1$. The corresponding input streams I_1 and I_2 are also shown. Here $x_1(t) > 0$ (or $x_2(t) > 0$) corresponds to logic output 1 and $x_!(t) < 0$ (or $x_2(t) < 0$) corresponds to logic output 0. The parameter values used for the simulation are $g = 0.1$, $\alpha_1 = 1.86$, $\alpha_2 = 0.325$, $\alpha_3 = 0.65$ and $\epsilon = 0.69$.

strengths was investigated [23]. It was found that the interplay of coupling and noise leads to the emergence of four distinct behavioural regimes. The first regime, where both coupling and noise are low, is characterized by no hops between wells and no synchrony between the two subsystems either. So both subsystems are very stable and remain in whatever well they evolve to from their initial states. The second type of behaviour arises for low coupling strengths and high noise strengths and is characterized by the subsystems switching between the wells, though this hopping is not synchronized. Thirdly, for strong coupling and weak noise, the two subsystems are synchronized and remain confined to the same well, that is we have synchrony without hopping. Lastly, for a specific range of noise and coupling strength, the coupled subsystems exhibit random hopping between the two wells in a synchronous manner, i.e. the two subsystems jump together from one well to another, a dynamical pattern that can be labelled synchronized hopping.

Further, in a recent advancement [24] it has been shown that in the regime of synchronized hopping, highly reliable logic response can be obtained when the input signals (I_1 and I_2) are separately fed into two coupled bistable subsystems with sufficient coupling strengths in an optimal window of noise. Since the signals are fed into individual subsystems, the coupling between them is pivotal here in obtaining the desired logical response. We implement the aforementioned *coupling induced LSR* using this memristive circuit to demonstrate another configuration in which consistent logic can be obtained.

3.1 Computational model

We computationally model this coupled system, where each individual unit is given by eq. (2), by the following

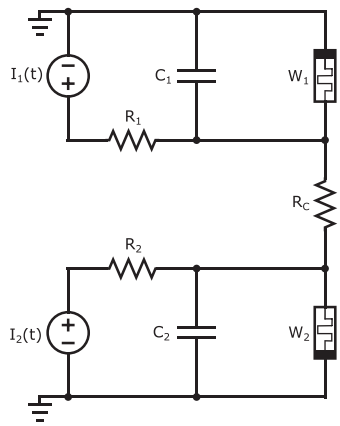


Figure 7. Schematic of the coupled memristive circuit. The circuit parameters are fixed as: $R_1 = R_2 = 2.4$ kΩ, $C_1 = C_2 = 10$ nF and coupling resistance $R_c = 5.57$ kΩ. The equivalent circuit for memristors W_1 and W_2 are same as elaborated in figure 1b.

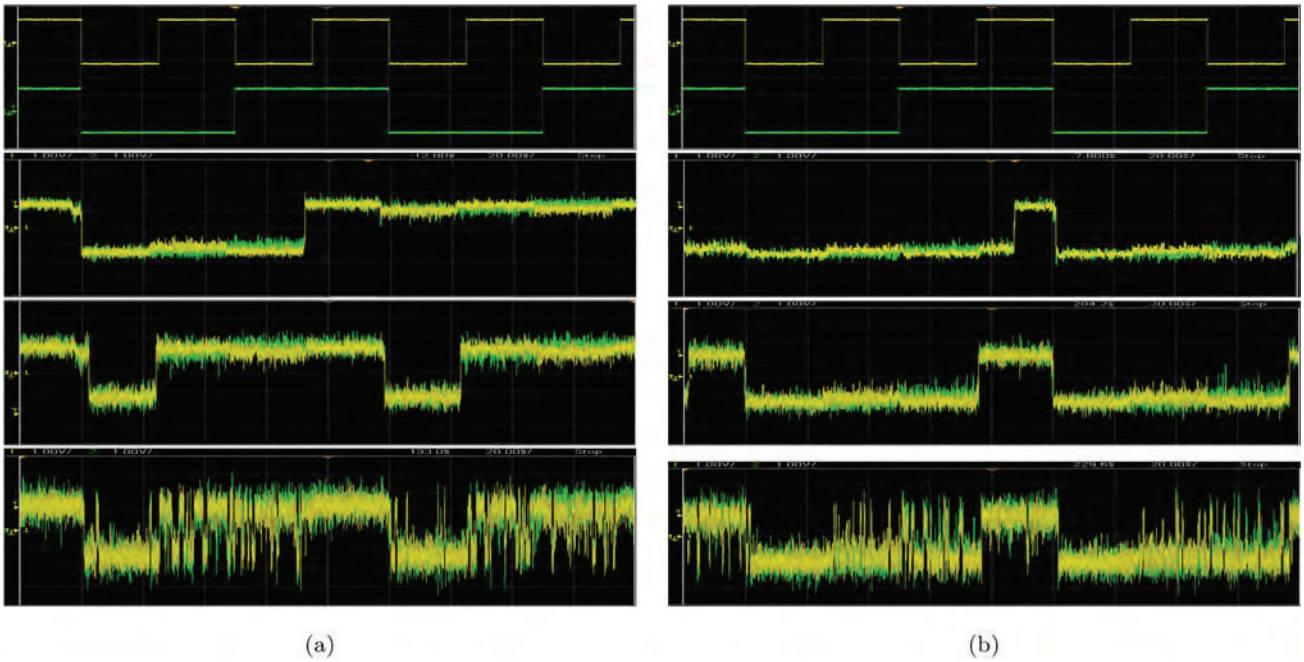


Figure 8. Waveforms obtained from hardware implementation of the coupled memristive circuit, showing the voltage across capacitors C_1 (yellow) and C_2 (green) for different noise levels: $D = 1$ V (second) $D = 1.8$ V (third) and $D = 2.8$ V (bottom); noise bandwidth 18 kHz (cf. figure 7). The top panel shows the two input streams I_1 (yellow) and I_2 (green). I_1 and I_2 take value -0.5 V when logic input is 0 and value +0.5 V when logic input is 1. Here the bias b is set to (**a**) $b = +150$ $\mathrm{mV_{pp}}$ and (**b**) $b = -150$ $\mathrm{mV_{pp}}$. Clearly the third panel (moderate noise) yields a consistent OR logic output for (**a**) and AND logic output for (**b**). The noise signal is drawn from Agilent or Keysight 33522A, Function/Arbitrary Waveform Generator. The oscilloscope used is Agilent or Keysight DSOX2012A. The scale of the traces is 1 V/Div (Y-axis) and 20 mS/Div (X-axis).

non-dimensionalized circuit equations:

$$\begin{aligned}
\dot{x_1} &= f_x(x_1, y_1) + I_1(t) + b + D\eta_1(t) + c(x_2 - x_1)\\
\epsilon\dot{y_1} &= f_y(x_1, y_1)\\
\dot{x_2} &= f_x(x_2, y_2) + I_2(t) + b + D\eta_2(t) + c(x_1 - x_2)\\
\epsilon\dot{y_2} &= f_y(x_2, y_2).
\end{aligned} \tag{3}$$

Here, c denotes coupling strength, D denotes the noise strength and b is a constant bias. η_1 and η_2 are uncorrelated Gaussian noises with mean zero and variance 1. The inputs I_1 and I_2 are used to drive the individual subsystems.

Figure 6 shows the time-series of the two state variables of the subsystems (x_1 and x_2), superposed with the expected logical outcomes for both AND and OR logic. We again observe that consistent logic response is obtained for a moderate noise strength while the consistency is lost both at high and low values of noise. We also observe that both x_1 and x_2 yield the same logic and

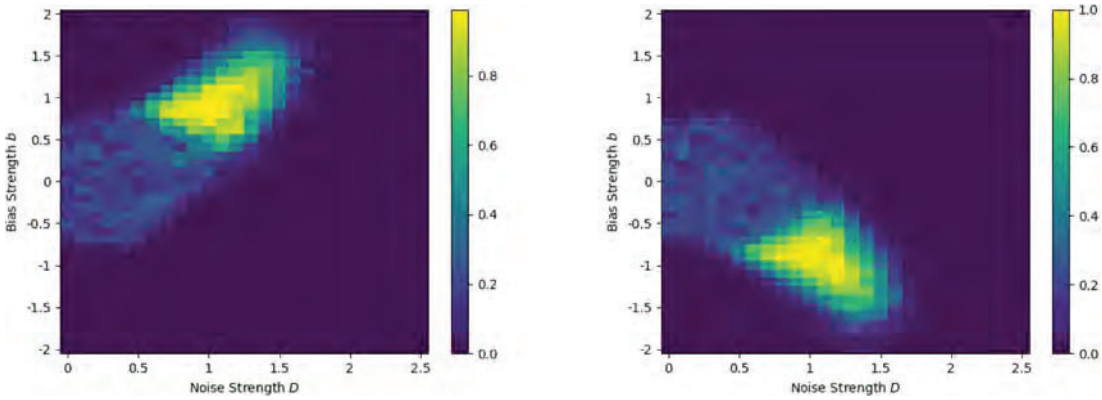


Figure 9. Dependence of the probability of obtaining (top) OR logic operation, P(OR) and (bottom) AND logic operation P(AND), on noise strength D and bias strength b, for coupling strength $c = 1$ and system parameters: $g = 0.1$, $\alpha_1 = 1.86$, $\alpha_2 = 0.325$, $\alpha_3 = 0.65$ and $\epsilon = 0.69$ in eq. (3).

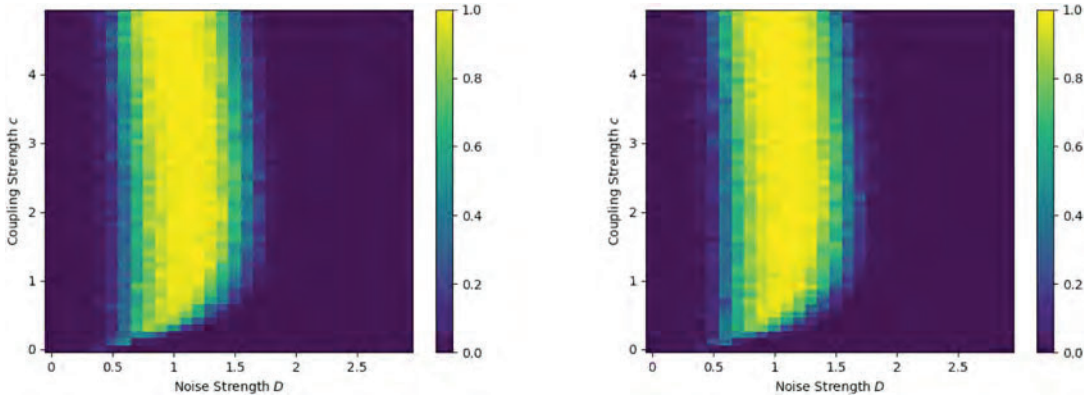


Figure 10. Dependence of the probability of obtaining (top) OR logic operation, P(OR) and (bottom) AND logic operation P(AND), on noise strength D and coupling strength c, for bias $b = 1$ and system parameters: $g = 0.1$, $\alpha_1 = 1.86$, $\alpha_2 = 0.325$, $\alpha_3 = 0.65$ and $\epsilon = 0.69$ in eq. (3).

consistent output can be obtained from either of them. This is a non-trivial feature, as one memristor receives input I_1, while the other receives input I_2. However, the output as determined by either state variable x_1 or x_2 is a logic function of both I_1 and I_2. Further, due to the inherent symmetry of the memristive circuit the other variables y_1 and y_2 yield the complementary logic i.e. if $b = -1$, while x_1 and x_2 produce AND logic, y_1 and y_2 yield NAND.

3.2 Experimental verification

To solidify the above computational result, we construct two identical copies of the memristive circuit, resistively couple them and demonstrate the occurrence of coupling induced LSR. The schematic circuit diagram of the construction is shown in figure 7. Here the active voltage controlled memristor W is the same as shown in figure 1b.

The oscilloscope trails of the voltage across capacitors C_1 and C_2 are shown in figure 8. It is evident that the experimental results are completely consistent with those observed in numerical simulations.

3.3 Quantitative measure of reliability

We again quantitatively identify the regions of parameter space where reliable logic operations occur, using the same rigorous metric described in section 2.3. Specifically, we use P(logic) to demarcate the regions in parameter space where logic operations are obtained consistently. In figure 9 we see that a broad range of noise (D) and bias (b) strengths yield completely reliable logic operations (i.e. P(logic) ~ 1), with positive values of bias yielding OR/NOR logic and negative values of bias yielding AND/NAND logic. Figure 10 shows the regions of reliable operation in the c–D space. Note that there exists a clear band of noise strengths for which consistent operations is obtained. Also, we observe the existence of a minimum threshold of coupling strength c for consistent operation. Coupling strengths larger than this threshold yields faithful logic. We did not find any upper bound in coupling strength c for obtaining P(logic) ≈ 1, in the explored range of $c \in [0, 5]$.

Further, it is interesting to note from figure 10 the behaviour of the window of optimal noise strengths for different values of coupling strength c. To make the behaviour more apparent, in figure 11 we show the minimum value of noise strengths D(low) required to produce consistent logic and the maximum value of noise strengths D(high) up to which consistent logic is produced. On increasing coupling strength c, we observe that both D(low) and D(high) show a sharp transition at a critical value, from zero to a finite moderate value, after which it saturates, with D(high) saturating

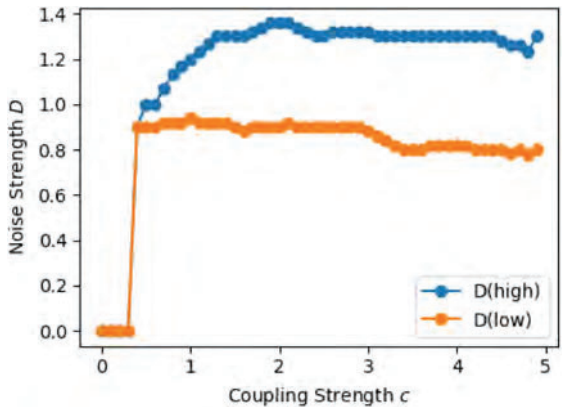


Figure 11. Dependence of the minimum noise strength (D(low)) and maximum noise strength (D(high)) required to obtain a probability P(logic) > 0.9 on the coupling strength c. Here the bias $b = +1$.

slower and at higher coupling strengths than D(low). So the width of the noise window supporting robust logic operations increases very sharply from zero after a critical coupling threshold and then rapidly saturates at increasing coupling strengths. This clearly indicates that coupling is crucial for obtaining reliable logic outputs, as robust operations are obtained only after sufficiently strong coupling.

4. Conclusions

We have implemented logic gates, in a second order autonomous memristive circuit, in the presence of a noise-floor. We have demonstrated that in an optimal band of noise one obtains logic operations extremely reliably. Additionally, the system yields the complementary logic operation in parallel as well. Lastly, the outputs can also be morphed to different logic functions by a simple switch of the constant bias. Furthermore, we also demonstrated the successful implementation of coupling induced LSR in a coupled system of memristors, and this paves the path for realization of multi-input logic gates without the need of separate adder circuits. All these ideas are demonstrated explicitly through numerical simulations, as well as proof-of-principle circuit experiments. Our demonstrations include stringent reliability tests, through estimations of a reliability measure obtained by extensive runs over a large number of samples, examining responses to randomly changing input streams, conducted over long runs to determine the stability of the outcome.

In summary, we have chosen to demonstrate noise-aided logic operations in a memristive circuit, as it has potential relevance for emerging new computing platforms of memristor-based memcomputing. While the results here are at the proof-of-concept stage, they suggest that memristive circuits may offer a promising system to implement robust and flexible logic operations. Further developments focussing on reduction of power and space costs are of course necessary in order to assess the full potential of the core idea.

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